memory and to the integrated circuit alterable memory and generating product operands by multiplying communications operands in response to the instructions and

b) an integrated circuit adder circuit coupled to the integrated circuit read only memory and generating filtered operands by adding the product operands in response to the instructions; and

an integrated circuit output circuit coupled to the integrated circuit read only memory and generating output operands by outputting the filtered operands in response to the instructions.

--92. (Amended) An integrated circuit filter processor system as set forth in claim 87, wherein the integrated circuit alterable memory includes an integrated circuit dynamic random access alterable memory dynamically storing operands, said filter processor further comprising a refresh circuit coupled to the integrated circuit alterable memory and refreshing the integrated circuit alterable memory.

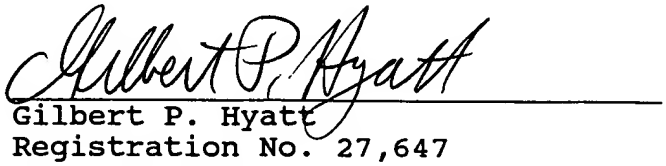
## IV SUMMARY

It is respectfully submitted that the present application meets the requirements of the patent laws (Title 35 USC), the patent rules (Title 37 CFR), and the Manual of Patent Examining Procedure and that all claims are patentably distinct over the prior art.

CERTIFICATION OF MAILING: I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231 on the date set forth below.

Respectfully submitted,

Dated: September 5, 1991



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